EXPRESS MAIL LABEL NO. EV731628510US
DATE MAILED: 09 JANUARY 2006

Attorney Docket No. SYNP 106

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent No. 6,434,733	
Patent Owner: Synopsys, Inc.	
Issued: August 13, 2002	Attn: Reexamination Group
Filed: March 24, 1999	**CUSTOMER NO. 36454**
For: **System and Method for High-Level Test Planning for Layout**	

REQUEST FOR EX PARTE REEXAMINATION BY PATENT OWNER

Mail Stop Ex Parte Reexam
Commissioner for Patents
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REQUEST FOR EX PARTE REEXAMINATION BY PATENT OWNER

TABLE OF CONTENTS

APPENDIX

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Sir:

Synopsys, Inc. ("Patent Owner"), the assignee of the above-captioned U.S. Patent No. 6,434,733 (the " '733 Patent", copy attached as "Exhibit A"), hereby submits a request for ex parte reexamination for claims 1 and 8 of the '733 Patent pursuant to 35 U.S.C. 302.

Ex parte reexamination may be requested at any time during the period of enforceability of a patent pursuant to 37 CFR 1.510(a). The '733 Patent has a filing date of March 24, 1999 and an issue date of August 13, 2002. Accordingly, the present request for ex parte reexamination is timely made during the period of enforceability of the '733 Patent.

Substantial New Question of Patentability

The '733 Patent is a subject of litigation before the U.S. District Court for the District of Delaware, styled "Synopsys, Inc. v. Magma Design Automation, Inc." case no. C.A. No. 05-701-GMS. Magma Design Automation, Inc. (hereinafter "Magma") alleged that two references anticipate or render obvious all the claims in the '733 patent, and that such references were not considered by the Examiner during the prosecution of the '733 Patent. "Answer to Complaint and Counterclaims" (copy attached as "Exhibit B"), page 13, paragraph 67 and paragraph 69.

The two references referred to by Magma include Barbagallo *et al.*, "Scan Insertion Criteria for Low Design Impact", Proc IEEE VLSI Test Symposium, 1996 (hereinafter "Barbagallo 1," copy attached as "Exhibit C") and Barbagallo *et al.*, "Layout-driven scan chain partitioning and reordering", IEEE European Test Workshop, 1996 (hereinafter "Barbagallo 2," copy attached as "Exhibit D"). Barbagallo 1 and Barbagallo 2 are prior art printed publications under 35 U.S.C. 102(b). Form PTO/SB/08B is attached as "Exhibit E," listing Barbagallo 1 and Barbagallo 2.

The substantial new question of patentability is whether, or not, any claim in the '733 Patent is anticipated or unpatentable in view of the Barbagallo 1 and Barbagallo 2.

The question is "new" because Barbagallo 1 and 2 have not been considered by the Patent and Trademark Office in connection with the '733 Patent.

The question is "substantial" because Magma has alleged in the above-referenced litigation that Barbagallo 1 and 2 anticipate all the claims in the '733 Patent. Because of Magma's allegations, there is a substantial likelihood that a reasonable examiner would consider the question important to deciding patentability. Manual of Patent Examining Procedure § 2642, Revision 3 of Eighth Edition, 2005.

The '733 Patent

The '733 Patent relates to EDA (Electronic Design Automation), a computer software system designers use for designing integrated circuit (IC) devices. The EDA system typically receives a description of an IC device in a language like VHDL, Verilog, etc., and translates the description into a netlist. The description is converted into a netlist by using a computer implemented synthesis process. A netlist is a description of the electronic circuit which specifies what cells compose the circuit and which pins of which cells are to be connected together using interconnects. A scan insertion tool replaces memory cells of the netlist with scannable memory cells that are specially designed to apply test vectors or patterns to, and observe test vectors or patterns from, portions of the integrated circuit. In addition, the scan insertion tool links groups of scannable memory cells into scan chains so that the test vectors can be cycled into and out of the integrated circuit design. The scannable netlist does not specify physical design information including where the scannable memory cells are placed on a circuit board or silicon chip, or where the interconnects for the scan chains run. Determining this physical design information is the function of a computer controlled layout process. '733 Patent, columns 1 and 2.

The '733 Patent describes an embodiment of a "scan chain partitioning process". '733 Patent, column 6, lines 49-50. A scan chain partitioning process described in the '733 Patent "partitions the scan chain based on clock domains, edge sensitivity types, skew tolerance levels, BIST (Built-In Self Test) cone logic feeding, and SSO (Simultaneous Switching Output) requirements of the scan cells." '733 Patent, column 6, line 64 to column 7, line 1. "[T]he data representative of the sets of re-orderable scan cells ... is referred to as "partitioning information"". '733 Patent, column 6, line 64 to column 7, line 5. "[P]artitioning criteria (e.g., skew tolerance levels, edge sensitivity types, etc.) are applied to a scan chain to generate partitioning information specific to a scan chain, which is, in turn, provided to the layout processes as re-ordering limitations." '733 Patent, column 10, lines 63-67. "Once the sets are created, layout can reorder memory elements within the set." '733 Patent, column 11, lines 45-46. "The placement locations and wire geometry are optimized for the scan cells contained in the same set, and this is done for each set separately." '733 Patent, column 7, lines 22-24.

Prior Art

The background of the '733 Patent describes the layout process of the prior art. The layout process "in some cases may break up the scan chains and place the scan cells in such a way that the layout of the mission mode circuitry is not affected." '733 Patent, column 3, lines 5-8. The layout process "then reconnects the scan chain based on the placement of the scan cells. This process is also known as placement-based scan chain re-ordering." '733 Patent, column 3, lines 9-10.

The publications cited herein, Barbagallo 1 and 2, describe a type of placement-based scan chain re-ordering, which includes a scan insertion tool that executes a procedure for "organizing the global scan chain structure." See, Barbagallo 1, page 1, column 2, lines 3-12 of "Exhibit C" print. The Barbagallo scan insertion tool procedure includes techniques for partitioning scan cells in a design into a "predefined number of chains," based on parameters such as clock domain and the number of scan chains provided by the user. See, Barbagallo 1, page 1, column 2, line 38 to page 2, column 1, line 37 of "Exhibit C" print; Barbagallo 2, page 2, lines 35 to page 3, line 7 of "Exhibit D" print.

The Barbagallo scan insertion tool procedures are similar to those described in U.S. Patent No. 5,828,579 by Beausang et al. (hereinafter "Beausang," copy attached as "Exhibit F"), which was cited and considered by the Patent Office to determine the patentability of the

claims of the '733 Patent. See, "References Cited" on face of '733 Patent. Just as in Barbagallo 1 and 2, Beausang also describes a scan insertion tool procedure which includes techniques for partitioning scan cells in a design into a predefined number of chains, based on parameters such as clock domain and a parameter indicating the number of scan chains provided by the user. Beausang, column 9, lines 64-67; column 10, line 65 to column 11, line 4; column 17, lines 26-30; column 18, lines 44-51.

Application of the Cited References Against the '733 Patent

The claim chart on the following page applies the cited references (Barbagallo 1 and Barbagallo 2) against the independent claims of the '733 Patent.

U.S. Patent No. 6,434,733 Claim Limitations	Disclosure by References
1. A computer implemented process for electronic design automation, said process comprising the steps of:	
receiving an HDL description of an integrated circuit design;	NOT DESCRIBED Barbagallo 1 and 2 perform synthesis on a netlist.
generating a scannable netlist based on said HDL description, said scannable netlist comprising a scan chain;	NOT DESCRIBED Barbagallo 1 and 2 generate a scannable netlist based on a netlist.
partitioning said scan chain into a plurality of sets of re-orderable scan cells, wherein partitioning information which describes the scan cells of each set is generated; and	NOT DESCRIBED: The concept of partitioning a scan chain in a scannable netlist into sets is not described. Barbagallo 1 and 2 do not generate "said partitioning information."
based on said partitioning information, re-ordering scan cells of said scan chain during layout processes of said integrated circuit design, said step of re-ordering only re-ordering scan cells of a same set and not re-ordering scan cells of different sets.	NOT DESCRIBED: Barbagallo 1 and 2 apply placement-based scan chain re-ordering to the scan chains without use of "said partitioning information".
8. A computer controlled electronic design automation system comprising:	
a scan-insertion system for receiving an HDL description of an integrated circuit design and for generating a scannable netlist based on said HDL description, wherein said scan-insertion system inserts a scan chain of scan cells in said integrated circuit design;	NOT DESCRIBED Barbagallo 1 and 2 generate a scannable netlist based on a netlist.
a scan chain partitioning system for partitioning said scan chain into a plurality of sets of re-orderable scan cells and for reporting partitioning information indicative thereof; and	NOT DESCRIBED: The concept of partitioning a scan chain in a scannable netlist into sets is not described. Barbagallo 1 and 2 do not report "partitioning information."
a place-and-route system for generating a layout from said scannable netlist, said place-and-route system for re-ordering said scan cells of said scan chain based on said partitioning information by re-ordering scan cells of a same set and not re-ordering scan cells of different sets.	NOT DESCRIBED: Barbagallo 1 and 2 do not generate "said partitioning information."

Conclusion

In light of the allegations made by Magma in the above-referenced litigation, a "substantial new question of patentability" has been raised against the '733 Patent. However, claims 1 and 8 of the '733 Patent include multiple claim limitations which are not disclosed by the cited references, separately or in combination.

The standards for construing claims are different during litigation and reexamination. In re Yamamoto, 740 F.2d 1569,1572 (Fed. Cir. 1984). During reexamination, the claims are not presumed valid, and the Patent Office uses a broadest reasonable interpretation approach in construing the claims. Because Courts may use different standards in construing patent claims, and may not necessarily apply the broadest reasonable interpretation approach of a reexamination, Patent Owner does not admit that any aspect of any claim construction discussed in this request is necessarily applicable in any litigation or adopt any claim construction for purposes of litigation. This request is for purposes of reexamination only, and shall not be used in support of or opposition to any claim construction by any party to any litigation.

Fee Authorization. The Commissioner is hereby authorized to charge underpayment of any additional fees or credit any overpayment associated with this communication to Deposit Account No. 50-0869 (SYNP 106).

Respectfully submitted,

Attorneys for Patent Owner

Date: 9 Jan 06

By: _____
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